QUINTUPLE MODULAR REDUNDANCY FOR HIGH RELIABILITY CIRCUITS IMPLEMENTED IN PROGRAMMABLE LOGIC DEVICES

ABSTRACT

Structures and methods for generating high reliability designs for PLDs on which single event upsets have minimal impact. When standard triple modular redundancy (TMR) methods are used in PLDs, a single event upset can short together two module output signals and render two of the three voting circuit input signals invalid. The invention addresses this issue by providing quintuple modular redundancy (QMR) for high-reliability circuits implemented in PLDs. Thus, a single event upset that inadvertently shorts together two PLD interconnect lines can render invalid only two out of five module output signals. The majority of the five modules still provide the correct value, and the voting circuit is able to correctly resolve the error. In some embodiments, a user selects a high-reliability circuit implementation option and/or a PLD particularly suited to a QMR implementation, and the PLD implementation software automatically implements the QMR structure for the user circuit.